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PERFORMANCE ANALYSIS OF CACHE MEMORY DESIGN FOR SINGLE BIT ARCHITECTURE FOR ULTRA-LOW POWER

Varun Dixit[1] & Apoorva Mishra[2]

[1]Senior Member of Technical Staff at Omnissa LlC,

[2]Independent Researcher

ABSTRACT

In this paper, the design analysis of ultra-low-power cache memory design for single-bit architecture has been proposed and implemented. Cache Memory Design for Single Bit Architecture is composed of a circuit of the write driver circuit, six transistors static random access memory cell, and different types of sense amplifiers such as voltage differential sense amplifier, current differential sense amplifier, and charge transfer differential sense amplifier. Power reduction techniques are also applied over different blocks of architecture, such as sense amplifiers and six transistors static random access memory cells. The performance of different architectures has been analyzed in terms of power consumption, the number of transistors,and delay in sensing. The results depicted that single-bit six transistor static random access memory cell voltage mode differential sense amplifier architecture consumes 13.16µW of power, 12.5ηs delay in sensing, with 30 transistors compared to others. Furthermore, Process Corner Simulation and Monte Carlo Simulation also have been done to check the robustness of the circuit. The conclusion depicts that single bit six transistor static random access memory cell with power reduction sleep transistor technique voltage mode differential sense amplifier with power reduction sleep transistor technique in architecture consume 8.988 µW of power with 34 number transistors and lowest chip area 62.613× 30.48 mm2.

***KEYWORDS**: Six Transistor Static Random-Access Memory (6T-SRAM), Cache Memory Design for Single Bit Architecture (CMDSBA), Single Bit Six Transistor Static Random-Access Memory Current Differential Sense Amplifier Architecture (SB6TSRAMCDSAA), Single Bit Six Transistor Static Random Access Memory Charge Transfer Differential Sense Amplifier (SB6TSRAMCTDSAA),Single Bit Six Transistor Static Random Access Memory Voltage Differential Sense Amplifier (SB6TSRAMVDSAA).*

Article History

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1. INTRODUCTION

6T-SRAM is frequently used in microprocessors and on-chip system memory. 6T-SRAMs are utilized in a system-on-chip to store big caches on CPU cores and IPs such as graphics, audio, video, and image processing systems. 6T-SRAMs are used in high-performance graphics and microprocessors. 6 T-SRAMs, on the other hand, are utilized in processors for mobile, portable, and consumer devices, requiring comparatively minimal power. As 6T-SRAMs are used as large storage

systems on these devices, it is vital to maximizing their density.In some situations, up to 1024 6T-SRAM-bit cells are typically linked to the same bitlines to achieve the maximum density and array efficiency. Display sensor amplifiers are necessary for speed due to the high availability of the bit lines. Sensory amplifiers can read the data instead of waiting for the entire rail-to-rail swing by sensing a small differential voltage swing on the bit lines. A minimum amount of differential voltage on bit lines for reliability is required for conventional voltage sensing amplifiers. The time it takes for this differential voltage to be generated is based on bit capacity. The amount of dynamic power needed to precharge the bit lines is increased in direct relation to the required differential voltage.Because of the lower mobile and embedded CPU power needs, sensor amplifiers with less power than classic voltage differential sense amplifiermethods are needed.This paper compares the Single Bit Six Transistor Static Random-Access Memory Current Differential Sense Amplifier Architecture, Single Bit Six Transistor Static Random Access Memory Charge Transfer Differential Sense Amplifier, and Single Bit Six Transistor Static Random Access Memory Voltage Differential Sense Amplifier. CMDSBA has been proposed in the proposed work employing several SAs. Furthermore, power reduction (TPR) techniques such as power reduction dual sleep technique, power reduction forced stack technique, power reduction sleepy stack technique, and power reduction sleep transistor technique have been implemented.

1.1 Techniques of Power Reduction

In this section, a small introduction to power reduction techniques is discussed.

1.1.1 Power Reduction Dual Sleep Technique (PRDST)

Four transistors are utilized in this technique: PM0, PM1, and two NM0, NM1. In this approach, PM0 and NM0 are linked in parallel instead of the circuitry's voltage supply, while PM1 and NM1 are connected in parallel in the logic circuit in place of the ground [22]. PM0 and NM0 have the same input in this method, whereas PM1 and NM1 have the same information, as shown in Figure:1 (a).

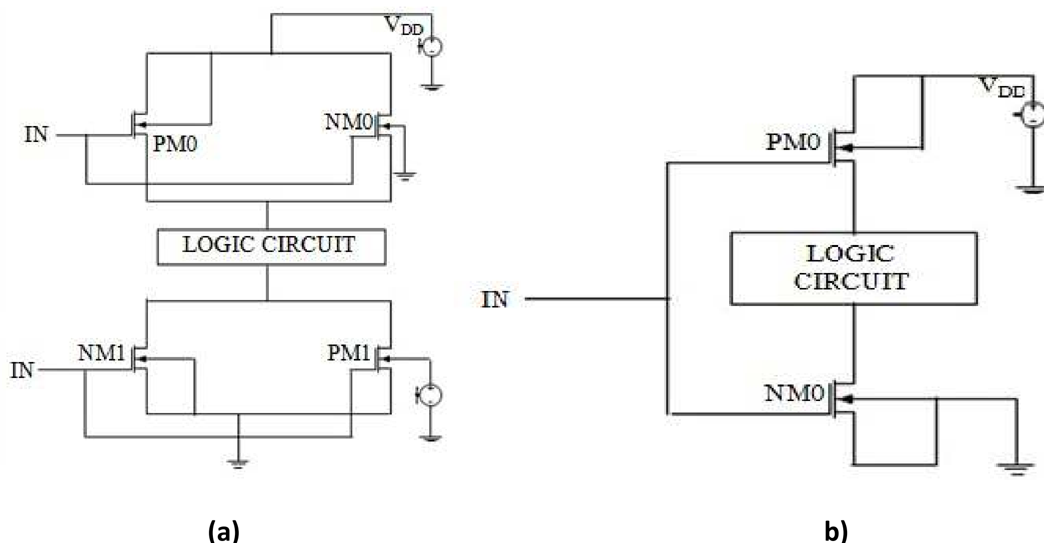


Figure: 1 (a) Power Reduction Dual Sleep Technique (b) Power Reduction Forced Stack Technique

1.1.2 Power Reduction Forced Stack Technique (PRFST)

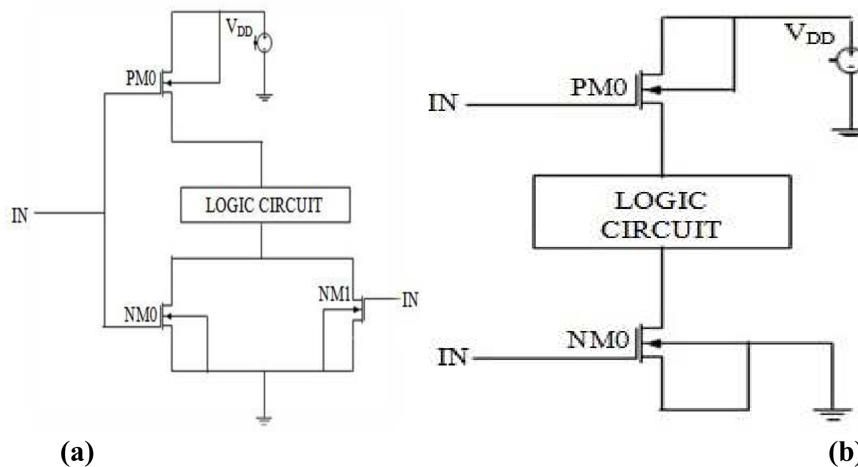
The forced stack approach uses PM0 instead of voltage supply and NM0 instead of ground in the logic circuit, as shown in Figure: 1 (b). Both mos have the same input in this approach. When PM0 is in the active zone, NM0 is in the cut-off region in this approach [19]. As a result, the circuit does not require constant power, resulting in lower power consumption.

1.1.3 Power Reduction Sleepy Stack Technique (PRFSST)

As illustrated in Figure 2, three transistors are utilized in this technique: PM0, NM0, and NM1 (a). Both NM0 and NM1 are linked in parallel in this approach. PM0 is utilized in place of the voltage supply, while NM0 and NM1 are used in place of the ground in the logic circuit [20]. PM0 and NM0 have the same input in this method, but NM1 has a separate input. PM0 is in the active region, NM0 is in the cut-off zone, and NM1 is in the activepart while the circuit is in operating mode. PM0 is in the cut-off area in standby mode, NM0 is in the active region, and NM1 is in the cut-off region [21].

1.1.1 Power Reduction SleepTransistor Technique (PRSTT)

Figure 1(a) shows that the sleep transistor technology is also a switching technique. Two transistors, PM0 and NM0, are switches in the sleep transistor method. Instead of a voltage source, PM0 is utilized in this approach, and NM0 is used in the logic circuit instead of the ground.When the logic circuit is in operation, PM0 is in the active area, and NM0 is also in the active region; however, when the circuit is in standby mode, PM0 is in the cut-off region, and NM0 is also in the cut-off region, resulting in a lower power consumption [17, 18].



(a) **(b)**

Figure: 2(a) Power Reduction Sleepy Stack Technique (b) Power Reduction Sleep Transistor Technique

PM0 is in the active region, NM0 is in the cut-off area, NM1 is in the active part, and PM1 is in the cut-off region while the circuit is in operating mode [23]. PM0 is in the cut-off area, NM0 is in the active part, NM1 is in the cut-off region, PM1 is in the active region while the circuit is in standby mode. As demonstrated in Figure: 2 (b) [24], our circuitry uses less power.Apart from the introduction, Section II covers the purpose and history of a single-bit cache memory design andeach Block's circuitry and working mechanism. Section III explained the suggested circuit architecture with output waveforms and comparisons. In Section IV, the conclusion has been described.

Section II

1. Literature Review

Sense amplifiers must work fast while using the least possible power, depending on the performance and power requirements.The high-bit line capacitance is a significant performance limit. Table:1 describe work done by different authors from 2002 to 2011.

Table 1: Work done by different authors from 2002 to 2011

Year	Author	Features	Sensing Delay	Supply Voltage
2002	Chrisanthopouloset al.	Conventional SA	7.1 ns	2.5V
2002	Chrisanthopoulos et al.	Clamped Bit Line SA	0.35 ns	2.5V
2002	K.S. Yeo et al.	Low power current SA	1.04 ns	2.0V
2002	Chrisanthopoulos et al.	Simple Four Transistor SA	1.85 ns	2.5V
2004	Chun- lung Hsu et al.	High-Speed SA	0.51 ns	1.8V
2005	Z. H. Kong et al.	Ultra-low power	1.46 ns	1.8V
2007	Sandeep Patilet al.	Self-Biased Charge-Transfer SA	0.723 ns	1.8V
2008	Ya-Chun Lai et al.	Latch Type SA	0.33 ns	1.8V
2008	Anh-Tuan Do et al.	Fully Current Mode SA	0.38 ns	1.8V
2008	Do Anh-Tuan et al.	High-Speed SA	0.26ns	1.8V
2011	Anh-Tuan Do et al.	Alpha Latch SA	0.566 ns	1V
2011	Anh-Tuan Do et al.	Decoupled SA	0.214 (ns)	1V

2. Cache Memory Design for Single Bit Architecture

The architecture is made up of threeBlockswith three differentialsense amplifier circuits as a circuit of write driver (CWD), 6T-SRAM cell, and sense amplifier (SA), as shown in Figure: 3[25]. It consists of six input pins and five output pins. CWD has two input pins (Word Enables (WE) and Data), two output pins, BTL and BTL_{BAR}, 6T-SRAM has a single input pin, a word line (WL), and two output pins, V_1 and V_2. On the other hand, SA is coupled through bit lines to the 6T-SRAM cell. SA has three YSEL input pins, P_{CH} (precharge) and Sense amplifier (SA_{EN}), and two output pins (V_3 and V_4).

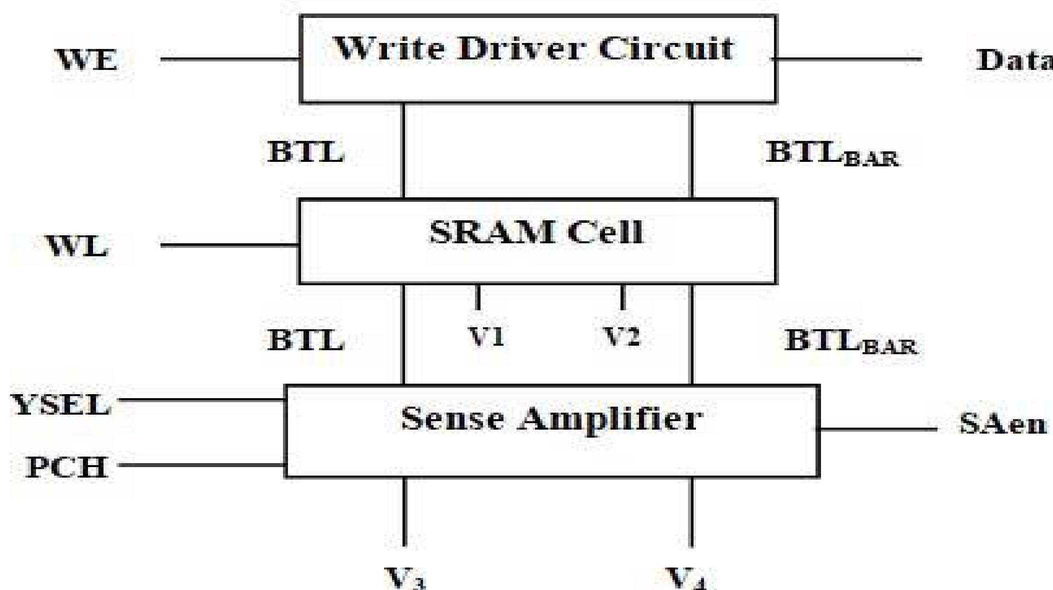


Figure 3: Block Diagram of Cache Memory Design for Single Bit Architecture

3.1 Circuit of Write Driver

In the 6T-SRAM cell, the CWD is utilized to save data. Figure: 4 shows a CWD scheme. CWD lowers the writing margin. The circuit has the task of loading or unloading the bit lines of the memory cell. Including PM1, PM2, PM3, PM4, PM5, NM1, NM2, NM3, NM4, and NM5, ten transistors include in a circuit. It consists of two WE and Data inputs and two BTL and BTL_{BAR} output pins linked to the 6T-SRAM cell input transistors.

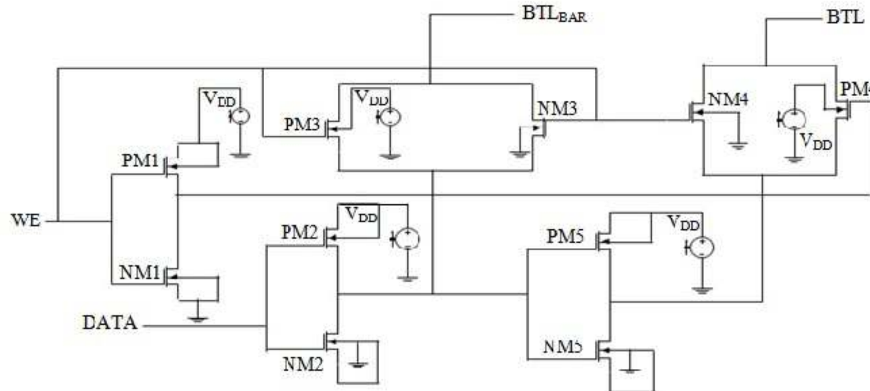


Figure: 4 Circuit of Write Driver Schematic.

3.2 6T-SRAMCell Schematic

In computers, 6T-SRAM is utilized as cache memory. It has a six-transistor configuration. As illustrated in Figure 5 [29], it has bistable (cross-coupled) inverters for storage (PM6, PM7, NM6, and NM7 function as crossed coupled inverters). The NM8 and NM9 access transistors are linked to BTL and BTL_{BAR} and are used to access stored data for reading and writing operations.

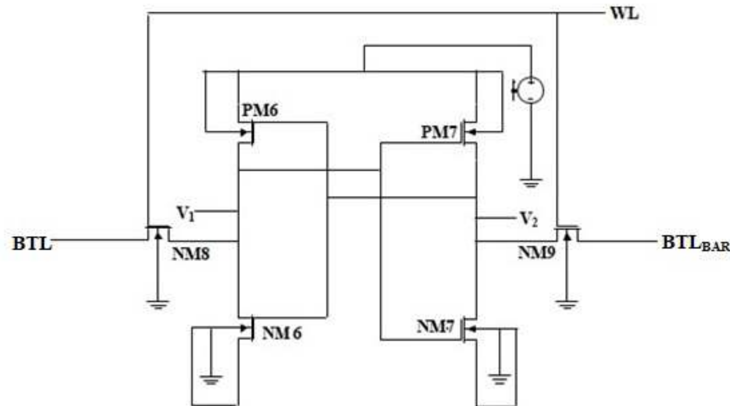


Figure 5: Schematic of 6T-SRAM Cell.

WL control access; when WL= low hold operation, so access transistors are off, data held in latch and when WL= high, read or write operation has been done, access transistors are turned ON,a voltage applied to BTL and BTL_{BAR}, data in latch overwritten with new value and BTL and BTL_{BAR} are read by SA's [30]. It is connected to the CWD and SA through BTL and BTL_{BAR}. When connected to the SA, resistance and capacitance are connected in parallel through BTLs [31].Memory cell transistor size affects 6T-SRAM performance and reliability. The architecture adopted for a cell should obey two basic rules for the proper functioning of 6T-SRAM.

- NM6 and NM7 pull-down network transistors must be approximately equal to or more potent than the access transistors (NM8 and NM9). This rule ensures read operation stability.
- The pull-up network transistors in PM6 and PM7 should be equal to or less than the access transistor (NM8 and NM9). This rule ensures that the value in the Bit-Cell is swapped during the writing process.

3.2 Sense Amplifier's

The SA is an important circuit in 6T-SRAM architecture. SA is used for a read operation in the 6T-SRAM cell. During reading operation BTL= low and BTL_{BAR}= high or BTL= high and BTL_{BAR}= low. This slow discharge of the bit cells BTL's capacitance and access transistor is small. Due to this, a small difference between bit lines is sensed and amplified by SA. The total width of the transistorshas been kept equal for all SAs. In this paper, three different types of amplifiers are used such as:

- Voltage Differential Sense Amplifier
- Current Differential Sense Amplifier
- Charge-Transfer Differential Sense Amplifier

SECTION III

4. Analysis of Result

Figure 6 Depicts a Single-Bit 6T-SRAM VDSA Architecture [25] Using CWD, a 6T-SRAM Cell, and VDSA as the SA.

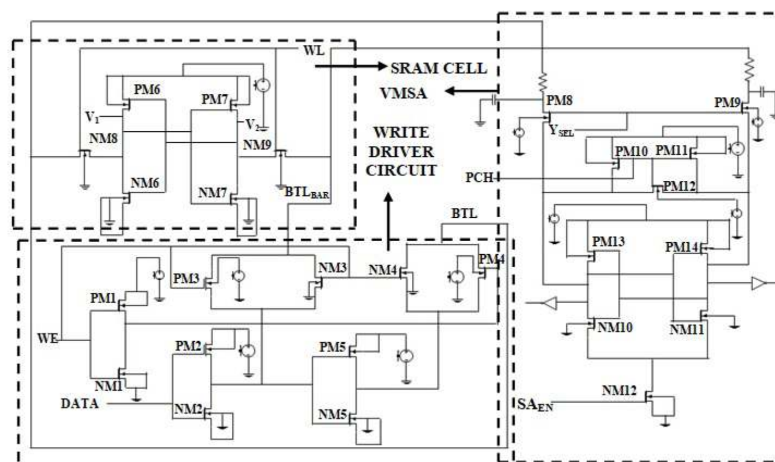


Figure 6: Schematic of Single Bit 6T-SRAM VDSA Architecture.

The BTLs and the SA output are both Pch high during the precharge period. Y_{SEL}= high, PCH= low, PM8, and PM9 are in the cut-off mode, while PM10, PM11, and PM12 are in active mode, and it Pch the BTL to the full rail swing, WL= low (no read operation), and SA_{EN} = low (no data sensed) since NM12 is in cut-off mode.

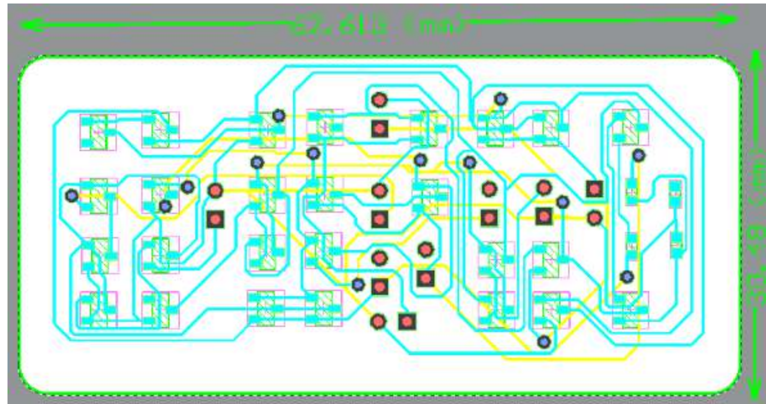


Figure 7: Single Bit 6T-SRAM VDSAArchitecture Chip Design.

Figure: 7 shows Single Bit 6T-SRAM VDSA Architecture Chip Design. Figure: 8shows the output waveform of CWD, where WE and DATA are inputs, and BTL and BTL_{BAR} are output in four cases. Here, H is denoted High, and L denotes Low.

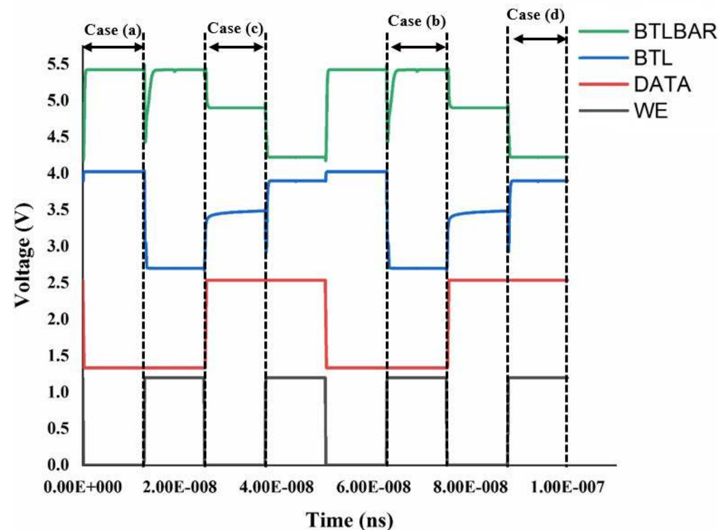


Figure 8: Circuit of Write Driver Output Waveform.

CASE 1: When WE = L and Data = L, BTL_{BAR} = H and BTL= H. PM1, PM2, and PM3 are in active mode while PM4 and PM5 are in cut-off mode NM1, NM2, NM3, NM4 are in cut-off mode while NM5is in active mode.

CASE 2: When WE= H and Data = L, BTLBAR = H and BTL= L. PM2 and PM4 are in active mode while PM1, PM3, and PM5 are in cut-off NM1, NM3, NM4, NM5 are in cut-off mode whileNM2 is in active mode.

CASE 3: When WE = L and Data = H, then BTL_{BAR} = H/2 and BTL = H/2. PM1, PM3, and PM5 are in active mode, while PM2 and PM4 are in the cut-off mode, NM2 is in active mode,and NM1, NM3, NM4, and NM5 are in cut-off mode.

CASE 4: When WE = H and Data = H, BTL_{BAR} = Land BTL = H. PM4 and PM5 are in active mode while PM1, PM2, and PM3 are cut-off, respectively, NM1, NM2, NM3, NM4 are in active mode whileNM5is in cut-off mode.

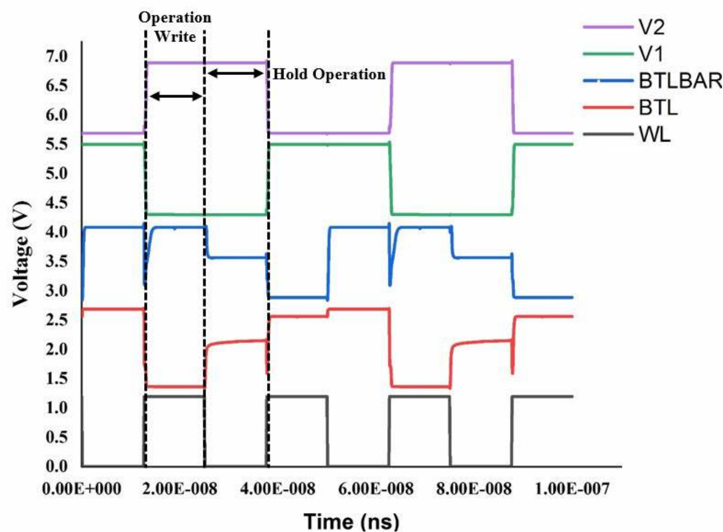


Figure 9: 6T-SRAM Cell Output Waveform.

The output waveform of the 6T-SRAM cell after both the write and hold operations have been held is shown in Figure: 9. The network (PM6 and PM7), pull-down network (NM6 and NM7), and access transistor (NM8 and NM9) all allow data to be stored and read by SA.

Figure:10 shows the Single Bit 6T-SRAM CDSA Architecture output waveform. During the evaluation phase: Y_{SEL} = low, Precharge circuits keep high to precharge the bit-lines (i.e., P_{ch} = high), PM8 and PM9 are in active mode, and data on the BTLs pass through while PM10, PM11, and PM12 are in the cut-off mode, WL of 6T-SRAM cell keeps high (i.e., WL = high) for reading operation, i.e., access transistors are turned ON, BTL= low and BTL_{BAR} = high, i.e., a voltage difference is high at the output (i.e., at V_3 and V_4), SA_{EN} = high for half positive cycle of WL at this time SA sense the difference between BTL and BTL_{BAR} and the stored data has been sensed as because NM12 is in active mode

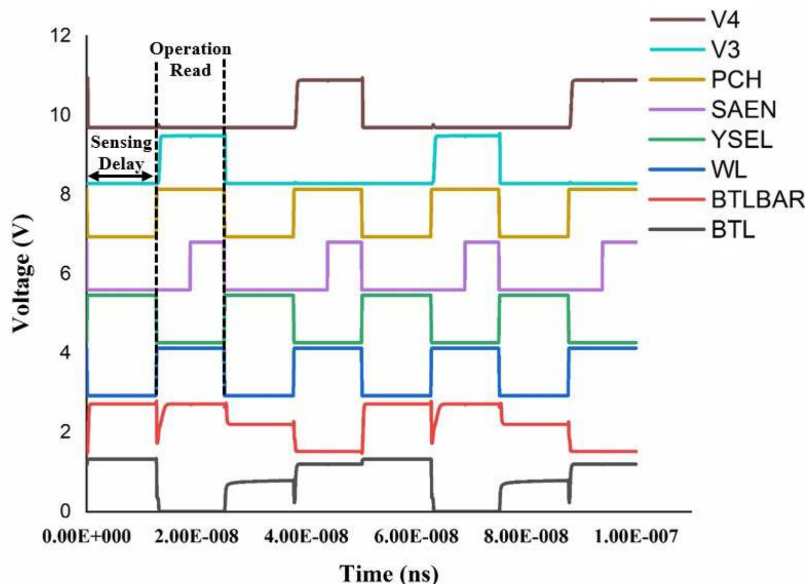


Figure 10: shows Single Bit 6T-SRAM VDSA Architecture Output Waveform

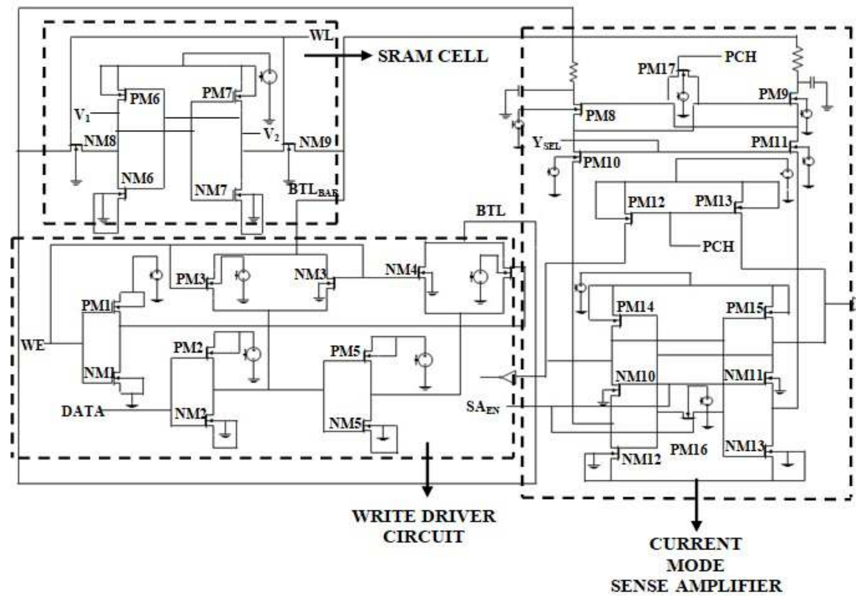


Figure 11: Single Bit 6T-SRAM CDSA Architecture Schematic.

Figure: 11 shows single-bit 6T-SRAM CDSA architecture composed of CWD, 6T-SRAMC, and VDSA.The description is divided into three different parts: a) the CWD with two input pins (word enable (WE) and bit) and two output pins (BTL and BTL_{BAR}), and b) the 6T-SRAM, which is attached to the CWD via bit lines (i.e., BTL and BTL_{BAR}), and an input pin (word line (WL) and two output pins (V_1 and V_2) and connected through bit lines having capacitance and resistance as a connector between them, c) CDSA which has five input pins (Y_{sel}, BTL, $BTL_{BAR,}$PCH, and SA_{EN}) and two output pins (V_3 and V_4).

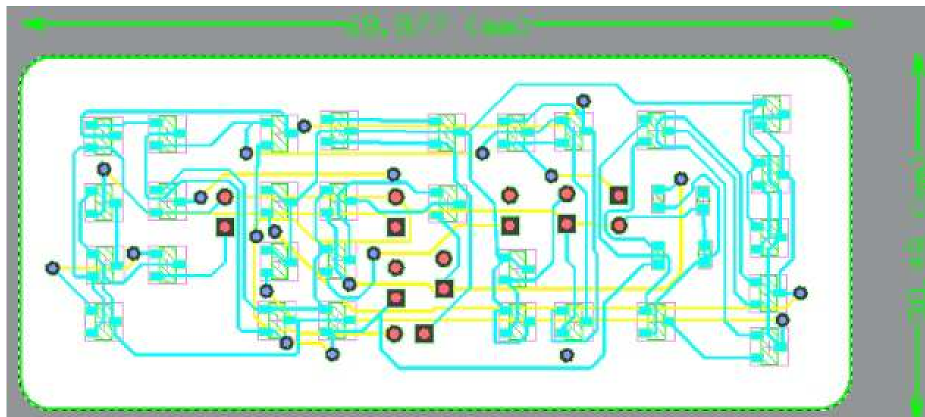


Figure 12: Single Bit 6T-SRAM CDSA Architecture Chip Design.

Figure:12 shows Single Bit 6T-SRAM CDSA Architecture Chip Design. Figure:13 shows the Single Bit 6T-SRAM CDSA Architecture output waveform, In the precharge phase: the bitlines and the output nodes SA_1 and SA_2 are P_{ch} high. Y_{sel}=V_{DD}, P_{ch}=0V, PM8and PM9 are in active mode due to while PM10 and PM11are in a cut-off way, due to which data at bit lines in the form of current is stopped at nodes SA_1 and $SA_2$and this charge the bit lines, and this causes nodes SA_3 and SA_4 to be pre-discharged to ground as because PM12 and PM13 are in active mode, WL=0V,i.e., no read operation and SA_{EN}=0V,i.e., SA does not sense any data as because NM10 and NM11 are in cut-off mode while PM16 is in active mode.

During the evaluation phase, Y_{SEL}=0, Precharge circuits keep high to precharge the BTLs (i.e., P_{ch}=V_{DD}), PM8

and PM9 are in the cut-off mode. The current on the bit-lines is passed through PM10, PM11 which is stored at nodes SA_1 and SA_2 as transistors are in active mode, while PM12 and PM13 are in a cut-off way, and the current is transferred to the nodes SA_3 and SA_4 through the drain of P_{mos} (PM10 and PM11), WL of 6T-SRAM cell keeps high(i.e., $WL=V_{DD}$) for reading operation, i.e., access transistors are turned ON, BTL= 0V and $BTL_{BAR}=V_D$), $SA_{EN}=V_{DD}$ (for half positive cycle of WL) at this time SA sense the difference between BTL and BTL_{BAR} and the stored data has been sensed as NM10 and NM11 are in active mode while PM16 is in cut-off mode due to which bias current flow through BTL and BTL_{BAR} of sense amplifier while PM16 keep the output equalized.

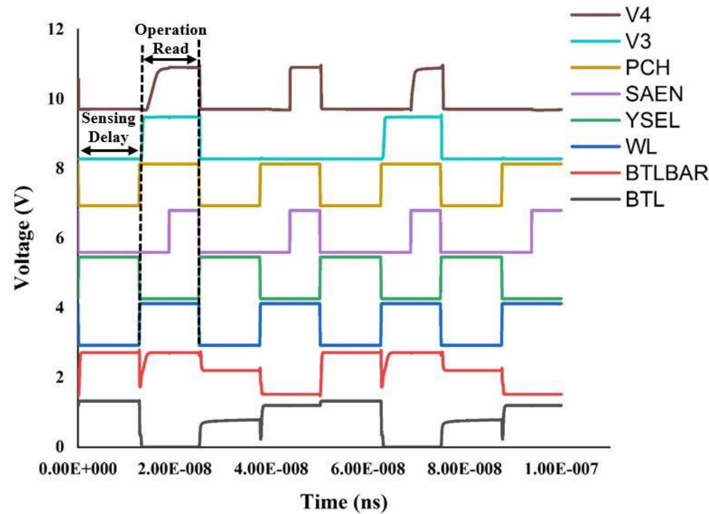


Figure 13: Shows Single Bit 6T-SRAM CDSA Architecture Output Waveform.

Figure 14: Shows a Single-bit 6T-SRAM CTDSA Architecture having CWD, 6T-SRAM cell, and CTDSA as a Sense Amplifier; the Working of this Circuit is the Same as Single Bit 6T-SRAMVDSA Architecture and Single-Bit 6T-SRAMCDSA Architecture.

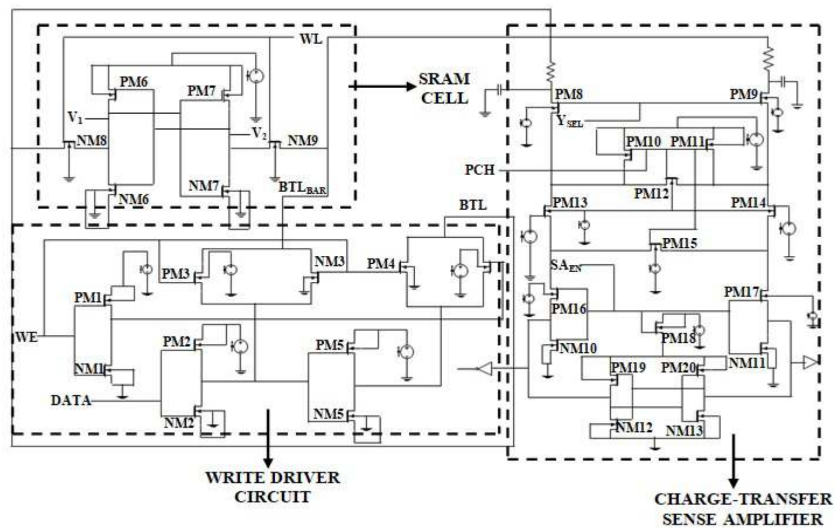


Figure: 14 Single Bit 6T-SRAM CTDSA Architecture Schematic.

The circuit is divided into two parts. In the first part, the common-gate cascade comprised PM13, PM16, and NM10 (and PM14, PM17 and NM12). The P_{mos} (PM13 and PM14) are biased at potential V_b. The second part, PM18,

PM19, PM20, NM12and NM13made cross-coupled inverters, latches the output of the common-gate amplifier (SA_1 and SA_2). In the precharge phase: the bit lines and all the internal nodes (SA_1, SA_2, SA_3, and SA_4) are pre-charged. $Y_{SEL}=V_{DD}$, $P_{ch}=0V$, PM8, and PM9 are in cut-off mode while PM10, PM11, and PM12 are in a playfulway, which precharge the bit lines to the V_{DD}, WL=0V,i.e., no read operation and $SA_{EN}=V_{DD,}$i.e., PM16, PM17, and PM18 are in cut-off mode while NM10 and NM11 is an active mode which precharge the bit lines at internal nodes at SA_5 and SA_6. During the evaluation phase: $Y_{sel}=0$, precharge circuits keep high to precharge the bit lines (i.e., $P_{ch}=V_{DD}$), PM8, andPM9 are in active mode. Data on the bitlines are passed from 6T-SRAM to SA at nodes SA_1 and SA_2. While PM10, PM11, and PM12 are in the cut-off mode, WL of the 6T-SRAM Cell keeps high (i.e., $WL=V_{DD}$) for reading operation, i.e., access transistors are turned ON, BTL= 0V, and $BTL_{BAR}=V_{DD,}$ i.e.,a voltage difference is V_{DD} at the output (i.e., at V_3 and V_4), $SA_{EN}=0V$ (for half positive cycle of WL) at this time SA sense the difference between BTL and BTL_{BAR} and the stored data has been perceived as because PM16, PM17, PM18 are in active mode BTL_{BAR} is started discharging. When the voltage of BTL_{BAR} goes to $V_b+|V_{t,\ p}|$, PM13 goes into the sub-threshold region. Whereas $BTL=V_{DD}$ charges the output nodes SA_5 to $V_{DD,}$ stored data can be sensed through V_3. Figure: 15 showsa single Bit 6T-SRAM CTDSA architecture chip design.

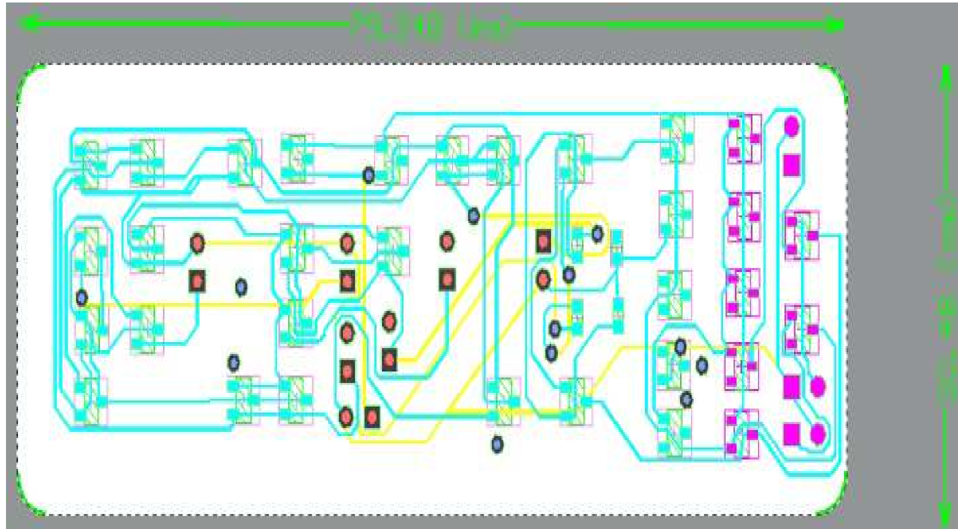


Figure: 15 Single Bit 6T- SRAM CTDSA Architecture Chip Design.

Figure:16 shows the output waveform of CTDSA, $Y_{SEL}=0$, precharge circuits keeps high to precharge the bit-lines (i.e., $P_{ch}=V_{DD}$), data on the bit-lines are passed from 6T-SRAM to sense amplifier, WL of 6T-SRAM cell keeps high (i.e., $WL=V_{DD}$) for reading operation, i.e., access transistors are turned ON, BTL= 0V and $BTL_{BAR}=V_{DD,}$ i.e., a voltage difference is V_{DD} at the output, $SA_{EN}=0V$ (for half positive cycle of WL) at this time sense amplifier sense the difference between BTL and BTL_{BAR} and the stored data has been sensed by the sense amplifier and stored is shown at $V_{4,}$ i.e., logic "1" is stored at the memory and hence sense by SA.

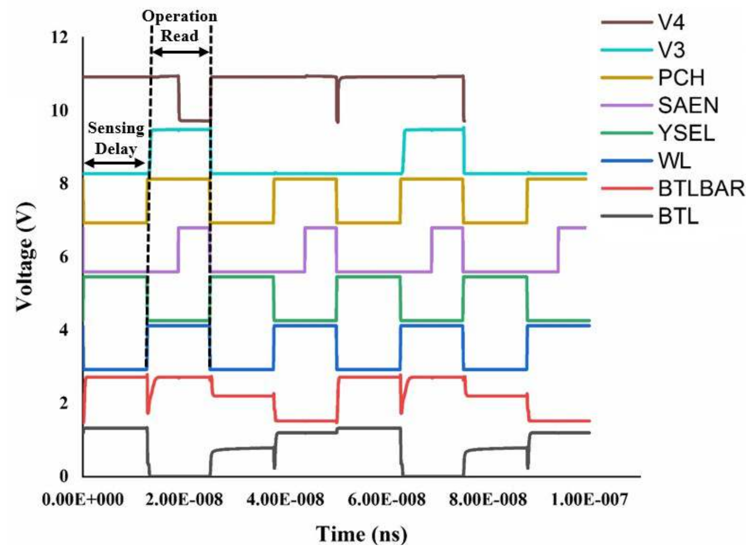


Figure 16: Shows Single Bit 6T-SRAM CTDSA Architecture Output Waveform.

Figure: 17 shows the Process Corner Simulation of Output V_3 of Sense Amplifier.

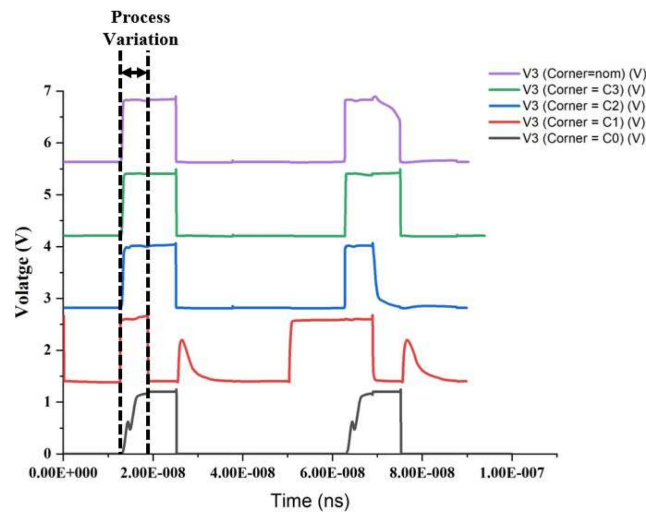


Figure: 17 Process Corner Variations

Five corners are shown in the figure as follows;

a) V3 (Corner=C3) significant that both N_{mos} and P_{mos} are slow (SS),

b) V3(Corner=C2) significant that both N_{mos} and P_{mos} are fast (FF),

c) V3(Corner=C1) significant that N_{mos} is fast and P_{mos} is slow (FS),

d) V3(Corner=C0) significant that N_{mos} and is slow P_{mos} is Fast (SF),

e) V3(Corner=nom) significant that both N_{mos} and P_{mos} have typical values (NN).

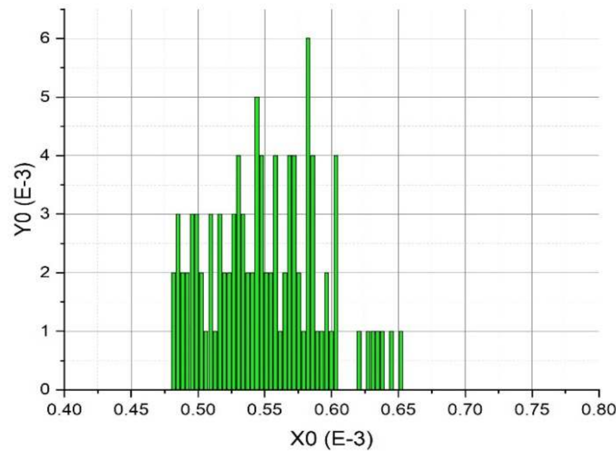


Figure: 18 Monte Carlo Simulations.

In this paper, there are tradeoffs between power consumption and area. Due to this region, different type of sense amplifiers has been analyzed to use the lowest power consumption, and different techniques are applied over 6T-SRAM and SA. Figure: 18 shows the Monte Carlo simulations of VTH_SAEN, on which the sense amplifier of a single-bit cache memory sense amplifier depends.

Table: 1 displays the various cache memory design parameters for a single-bit architecture. Different sense amplifiers are analyzed concerning their sensing delay parameter, and there is also an increase in area and a decrease in power. The conclusion is that the Single Bit 6T-SRAMC VDSA Architecture consumes 13.16 µWof power with 30 transistors in the design, giving low power consumption and less area.

Table: 1 Single Bit 6T- SRAM SA ArchitectureAnalysis of Different Parameters

Architectures	CP	NT
SB6T-SRAMVA	13.16 µW	30
SB6T-SRAMCA	16.44 µW	33
SB6T-SRAMCTA	44.63 µW	37

Total Power = Dynamic Power + Static Power (i.e., Total Power ≈ Dynamic Power)

If a reduction in static power does not much affect total power due to this reason, the main focus is on total power consumption.Due to this reason, power reduction techniques are applied instead of leakage power reduction techniques and also analyzed that there is no change in input and output of the design.

Table: 2 Single Bit6T-SRAM VDSA ArchitectureAnalysis of Different Parameters on Applying Techniques of Power Reduction over VDSA

S.No.	Architecture Techniques	SB6T-SRAMVA	
		CP	NT
1.	**PRSTT**	12.87 µW	32
2.	**PRFST**	13.03 µW	32
3.	**PRSST**	13.03 µW	33
4.	**PRDST**	12.88 µW	34

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAM VDSA Architecture (SB6T-SRAMVA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 2 describesthose techniques of power reduction applied over VDSA in Single Bit 6T-SRAM VDSA Architecture. There is reduced power consumption, which increases our circuit's working capacity. The conclusion arises that Single Bit 6T-SRAM VDSA with power reduction sleep transistor technique in Architecture consumes 12.87 µW of power with 32 transistors.

Table: 3 Single Bit6T-SRAM CDSA Architecture Analysis of Different Parameters on Applying Techniques of Power Reduction over CDSA

S.No.	Architecture Techniques	SB6T-SRAMCA	
		CP	NT
1.	PRSTT	14.28 µW	35
2.	PRFST	14.17 µW	35
3.	PRSST	14.82 µW	36
4.	PRDST	14.52 µW	37

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCDSA Architecture (SB6T-SRAMCA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 3 describes that applying power reduction techniques over CDSA in Single Bit 6T-SRAM CDSA Architectureto reduce consumption of power and concludes that single bit 6T-SRAM CDSA with power reduction forced stack technique in architecture consumes 14.17 µW of power with 35 transistors in design which increases area, i.e., ↓power consumption and ↑area.

Table 4 describes applying power reduction techniques over CTDSA in a Single Bit 6T-SRAM CTDSA Architecture to reduce power consumptionand concludes that single bit 6T-SRAM CTDSA with power reduction forced stack technique in architecture consumes 20.07 µW of power with 40 transistors in design.

Table 4: Single Bit6T-SRAM CTDSA Architecture Analysis of Different Parameters on Applying Techniques of Power Reduction over CTDSA

S.No.	Architecture Techniques	SB6T-SRAMCTA	
		CP	NT
1.	PRSTT	20.74 µW	39
2.	PRFST	20.74 µW	39
3.	PRSST	20.07 µW	40
4.	PRDST	21.74 µW	41

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCTDSA Architecture (SB6T-SRAMCTA), Consumption of Power (CP), Number of Transistor (NT)**

Table 5: Single Bit6T-SRAMVDSAArchitecture Analysis of Different Parameters on Applying Techniques of Power Reduction over 6T-SRAM

S.No.	TA6T-SRAMA	SB6T-SRAMVA	
		CP	NT
1.	PRSTT	9.39 µW	32
2.	PRFST	9.31 µW	32
3.	PRSST	11.50 µW	33
4.	PRDST	11.11 µW	34

*** Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAM VDSA Architecture (SB6T-SRAMVA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 5 describes applying power reduction techniques over 6T-SRAM in Single Bit 6T-SRAM VDSA Architectureto reduce power consumptionand concludes that single bit 6T-SRAM VDSA with power reduction forced

stack technique in architecture consumes 9.31 µW of power with 32 transistors in design.

Table 6: Single Bit6T-SRAM CDSA Architecture Analysis of Different Parameters on Applying Techniques of Power Reduction over 6T-SRAM

S.No.	TA6T-SRAMA	SB6T-SRAMCA	
		CP	NT
1.	PRSTT	13.62 µW	35
2.	PRFST	12.68 µW	35
3.	PRSST	14.14 µW	36
4.	PRDST	13.88 µW	37

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCDSA Architecture (SB6T-SRAMCA), Consumption of Power (CP), Number of Transistor (NT)**

Table 6 describes applying power reduction techniques over 6T-SRAM in Single Bit 6T-SRAM CDSA Architecture to reduce power consumptionand concludes that single bit 6T-SRAM CDSA with power reduction forced stack technique in architecture to consume 12.68 µW of power with 35 transistors in design.

Table 7 describes applying power reduction techniques over 6T-SRAM in Single Bit 6T-SRAM CTDSA Architecture to reduce power consumption and concludes that single bit 6T-SRAM CTDSA with power reduction dual sleep technique in architecture consumes 13.88 µW of power with 41 transistors in design.

Table: 7 Single Bit6T6T-SRAM CTDSA Architecture Analysis of Different Parameters on Applying Techniques of Power Reduction over 6T-SRA

S.No.	TA6T-SRAMA	SB6T-SRAMCTA	
		CP	NT
1.	PRSTT	14.14 µW	39
2.	PRFST	41.66µW	39
3.	PRSST	43.64 µW	40
4.	PRDST	13.88 µW	41

*** Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCTDSA Architecture (SB6T-SRAMCTA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 8 describes applying power reduction techniques over 6T-SRAM and VDSA in Single Bit 6T-SRAM VDSA Architectureto reduce power consumption and concludes that single Bit 6T-SRAM with power reduction sleep transistor technique VDSA with power reduction sleep transistor technique in architecture consumes 8.988 µW of power with 34 transistors in design.

Table 8 Single Bit6T-SRAM VDSA Architecture Different Parameters on Applying Techniques of Power Reduction over 6T-SRAM and VDSA

S.NO.	TA6T-SRAMA	SB6T-SRAMVA	
		CP	NT
1.	PRSTT	8.988 µW	34
2.	PRFST	9.332µW	34
3.	PRSST	9.331 µW	36
4.	PRDST	10.71 µW	38

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCTDSA Architecture (SB6T-SRAMVA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 9 describes applying power reduction techniques over 6T-SRAM and CDSA in Single Bit 6T-SRAM CDSA Architectureto reduce power consumption and concludes that single Bit 6T-SRAM with power reduction forced stack technique CDSA with power reduction forced stack technique in architecture consumes 12.52 µW of power with 37 transistors in design.

Table: 9 Single Bit6T-SRAM CDSA Architecture Different Parameters on Applying Techniques of Power Reduction over 6T-SRAM and CDSA

S.NO.	TA6T-SRAMA	SB6T-SRAMCA	
		CP	NT
1.	PRSTT	12.99 µW	37
2.	PRFST	12.52µW	37
3.	PRSST	14.03µW	39
4.	PRDST	13.52µW	41

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCTDSA Architecture (SB6T-SRAMCA), Consumption of Power (CP), Number of Transistor (NT)**

Table: 10 explains how to apply power reduction techniques to 6T-SRAM and CTDSA in Single Bit 6T-SRAM CDSA Architecture to reduce power consumption. It concludes that Single Bit 6T-SRAM with Power Reduction Forced Stack Technique CDSA with Power Reduction Forced Stack Technique in Architecture consumes18.15 µWof Power with 41 Transistors in Design.

Table 10: Single Bit6T-SRAM CTDSA Architecture Different Parameters on Applying Techniques of Power Reduction over 6T-SRAM and CTDSA

S.NO.	TA6T-SRAMA	SB6T-SRAMCTA	
		CP	NT
1.	PRSTT	18.15 µW	41
2.	PRFST	18.12 µW	41
3.	PRSST	19.20 µW	43
4.	PRDST	18.85 µW	45

***Techniques Applied over 6T-SRAM in Architecture (TA6T-SRAMA), Single Bit 6T-SRAMCTDSA Architecture (SB6T-SRAMCTA), Consumption of Power (CP), Number of Transistor (NT)**

5. CONCLUSIONS

Cache Memory Design for Single-Bit Architecture has been implemented with VDSA, CDSA, and CTDSA and compared in the proposed work. Architecture composed of Circuit of Write Driver, 6T-SRAMand SA's and different architecture has been analyzed such as Single Bit 6T-SRAM VDSA Architecture, Single Bit 6T-SRAM CDSA Architecture and Single Bit 6T-SRAM CTDSA Architecture in terms of consumption of power and number of transistors. Apart from optimizing power consumption, power reduction techniques have been applied to different architecture blocks. The result depicted that Single Bit 6T-SRAM with power reduction sleep transistor technique VDSA with power reduction sleep transistor technique in architecture consumesthe lowest power but area increases. All simulations have been done in 45nm CMOS technology on the cadence virtuoso tool. Furthermore, Process corner simulation and Monte Carlo simulation also have been done to check the robustness of the proposed design, and there is no variation of more than three percent. In the future, this work can be extended as an array.

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